FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.:	Applic. No.
P2001,0216	10/673,705

Applicant: Annalisa Cappellani et al.

Filing Date	Group Art Unit
September 26, 2003	

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
SBG	A	6,277,699 B1	08/21/01	Chen et al.	—	—	
	B						
	C						
	D						
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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	~~381309~~	~~09/19/98~~	~~Taiwan~~				~~X~~
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	
	P	

EXAMINER	DATE CONSIDERED
Fred B. Dy	6/7/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
SBG	A	6,091,120	7/18/00	Yeom et al.	—	—	
SBG	B	5,089,863	2/18/92	Satoh et al.	—	—	
SBG	C	5,384,479	1/24/95	Taniguchi	—	—	
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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
SBG	J	42 34 528 C2	4/15/93	Germany	—	—		X
SBG	K	42 34 777 A1	4/21/94	Germany	—	—		X
SBG	L	2 791 177 A1	9/22/00	France	—	—		
	M	~~63044768~~	~~2/25/88~~	~~Japan~~				
SBG	N	0 740 334 A2	10/30/96	Europe	—	—	X	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

SBG		Widmann, D. et al.: "Technologie hochintegrierter Schaltungen" [Technology of High-Density Integrated Circuits], Springer Verlag, 2nd Edition, pp. 201-203
SBG		Ghani, T. et al.: "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", IEEE, 1999, pp. 415-418

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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
SBG	J	0 328 350 A2	8/16/89	Europe	—	—	X	
SBG	K	02/41383 A1	5/23/02	WIPO	—	—	X	
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

SBG		Lasky, J. B. et al.: "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of $TiSi_2$ and $CoSi_2$", IEEE Transactions on Electron Devices, Vol. 38, No. 2, February 1991, pp. 262-269
SBG		Hisamoto, D. et al.: "A Low-Resistance Self-Aligned T-Shaped Gate for High-Performance Sub-0.1-μm CMOS", IEEE Transactions on Electron Devices, Vol. 44, No. 6, June 1997, pp. 951-956

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	K							
	L							
	M							
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

SBG		Kasai, K. et al.: "W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs", IEEE, 1994, pp. 497-500

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[signature]	6/7/04